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10/688,487	10/16/2003	Robert A. Rust	10991599-3	2149

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EXAMINER	
PUENTE, EMERSON C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,487	RUST ET AL.	
	Examiner	Art Unit	
	Emerson C. Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 have been cancelled. Claims 21-51 have been examined.

This action is made **Non-FINAL.**

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 21-23, 25, 28-30, 32, 33, and 39-41 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 10, 11 of U.S. Patent No. 6,647,516. Although the conflicting claims are not identical, they are not patentably distinct from each other.

In regards to claim 21, Patent '516 discloses:

storage circuitry configured to store digital data. Patent '516 discloses a "data storage system"(see claim 10; column 8 line 30).

a plurality of components coupled with the storage circuitry and configured to communicate transactions with respect to one another and to process the transactions to effect operations with respect to storage of digital data using the storage circuitry. Patent '516 discloses "a plurality of components configured to process transactions...providing the transactions for communication to respective components" (see claim 10; column 8 line 31-33).

wherein at least one of the components is configured to detect a presence of a fault in a transaction communicated from an other of the components. Patent '516 discloses "detecting error conditions within the transactions" (see claim 10; column 8 line 35), and

to disable communication of subsequent transactions from the other component to the one component after the detection of the transaction including the fault from the other component Patent '516 discloses "preventing entry of subsequent transactions received from one of the components"(see claim 10; column 8 lines 40-42).

With regard to the additional limitations in claim 10 of Patent '516, which are not included in the claim 21 of the application, the omission of these limitation in the claim 21 of the application is an obvious expedient since the remaining limitations in claim 10 of the Patent '516 perform the same function as the limitations in claim 21 of the application (*In re Karlson,* 136 USPQ 184 (CCPA 1963)).

In regards to claim 22, Patent '516 discloses:

wherein the one component is configured to not process the transaction including the fault. Patent '516 discloses "preventing entry of transactions which individually include an error condition" (see claim 10; column 8 lines 36-37)

In regards to claim 23, Patent '516 discloses:

wherein the storage circuitry comprises a plurality of redundant storage circuits configured to redundantly store digital data. Patent '516 discloses "a fault tolerant data storage system" (see claim 10; column 8 line 30)

In regards to claim 25, Patent '516 discloses:

wherein the one component is configured to disable an interface in communication with the other component to disable the communication of subsequent transactions. Patent '516 discloses "wherein the preventing entry comprises disabling interfaces of the respective components"(see claim 11; column 8 lines 45-46)

In regards to claim 28, Patent '516 discloses:

storage circuitry comprising a plurality of redundant storage circuits configured to redundantly store digital data. Patent '516 discloses "a fault tolerant data storage system" (see claim 10; column 8 line 30)

a plurality of components coupled with the storage circuitry and the components are configured to communicate transactions with respect to one another and to process received transactions to effect operations with respect to storage of digital data using the redundant storage circuits. Patent '516 discloses "a plurality of components configured to process transactions...providing the transactions for communication to respective components" (see claim 10; column 8 line 31-33).

wherein the components are individually configured to identify transactions which include a fault. Patent '516 discloses "detecting error conditions within the transactions" (see claim 10; column 8 line 35), and

to prevent processing of the transactions which have been identified as including a fault using the respective individual component. Patent '516 discloses "preventing entry of subsequent transactions received from one of the components"(see claim 10; column 8 lines 40-42).

With regard to the additional limitations in claim 10 of Patent '516, which are not included in the claim 28 of the application, the omission of these limitation in the claim 28 of the application is an obvious expedient since the remaining limitations in claim 10 of the Patent '516 perform the same function as the limitations in claim 28 of the application (*In re Karlson,* 136 USPQ 184 (CCPA 1963)).

In regards to claim 29, Patent '516 discloses:

wherein the transactions which include a fault are communicated from at least one of the components, and others of the components are configured to disable communications with respect to the one component to prevent the processing. Patent '516 discloses "providing the transactions for communication to respective components...preventing entry of transactions which individually include an error condition into respective components responsive to the detecting" (see claim 10; column 8 lines 33-37).

In regards to claim 30, Patent '516 discloses:

wherein the others of the components are individually configured to disable a respective interface coupled with the one component to disable the communications. Patent '516 discloses "wherein the preventing entry comprises disabling interfaces of the respective components"(see claim 11; column 8 lines 45-46)

In regards to claim 32, Patent '516 discloses:

wherein the components are individually configured to prevent the respective processing responsive to the identification. Patent '516 discloses "preventing entry of transactions which individually include an error condition" (see claim 10; column 8 lines 36-37)

In regards to claim 33, Patent '516 discloses:

wherein at least one of the components is configured to identify at least one of the transactions including a fault as being communicated from an other of the components and to prevent processing of subsequent transactions communicated from the other component after the identifying. Patent '516 discloses, "preventing entry of subsequent transactions received from one of the components received from one of the components responsive to the detecting "(see claim 10; column 8 lines 40-44).

In regards to claim 39, Patent '516 discloses:

storing digital data using a data storage system.Patent '516 discloses a "data storage system"(see claim 10; column 8 line 30).

communicating a plurality of transactions intermediate a plurality of components of the data storage system; processing the transactions using the components; using the components, effecting operations with respect to storage of digital data responsive to the processing. Patent '516 discloses "a plurality of components configured to process transactions...providing the transactions for communication to respective components" (see claim 10; column 8 line 31-33).

identifying one of the transactions from one of the components as including a fault, Patent '516 discloses "detecting error conditions within the transactions" (see claim 10; column 8 line 35);

disabling communications of others of the transactions from the one component responsive to the identifying. Patent '516 discloses "preventing entry of subsequent transactions received from one of the components"(see claim 10; column 8 lines 40-42).

In regards to claim 40, Patent '516 discloses:

wherein the storing digital data comprises redundantly storing digital data using a plurality of redundant storage circuits of the data storage system. Patent '516 discloses "a fault tolerant data storage system" (see claim 10; column 8 line 30)

In regards to claim 41, Patent '516 discloses:

disabling respective interfaces of the other components responsive to the identifying. Patent '516 discloses "wherein the preventing entry comprises disabling interfaces of the respective components"(see claim 11; column 8 lines 45-46)

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 27, 35, 36, 43, and 51 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In regards to claim 27, the limitation "wherein at least one of the subsequent transactions does not include a fault" is not disclosed in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In regards to claim 35, the limitation "wherein subsequent transactions communicated from the identified means for processing which would otherwise be processed are not processed" is not disclosed in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In regards to claim 36, the limitation "wherein the subsequent transactions individually do not include a fault" is not disclosed in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In regards to claim 43, the limitation "wherein the disabling comprises disabling communications of at least one of the others of the transaction not including a fault" is not disclosed in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In regards to claim 51, the limitation "wherein the at least some communications individually do not include a fault" is not disclosed in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21-52 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,574,849 of Sonnier et al. referred hereinafter "Sonnier".

In regards to claim 21, Sonnier discloses:

storage circuitry configured to store digital data (see column 7 lines 13-35);

a plurality of components coupled with the storage circuitry and configured to communicate transactions with respect to one another and to process the transactions to effect operations with respect to storage of digital data using the storage circuitry (see figure 1a and column 10 lines 35-43 and column 7 lines 13-35); and

wherein at least one of the components is configured to detect a presence of a fault in a transaction communicated from an other of the components, and to disable communication of subsequent transactions from the other component to the one component after the detection of the transaction including the fault from the other component. Sonnier discloses the CRC of each message is checked at destination as well as while in route to the destination (ex. at each router crossing), indicating detecting a presence of a fault in a transaction communicated from an other of the components (see column 5 lines 35-40). He further discloses isolating a link or a router element that introduces an error, indicating disabling communication of subsequent transactions from the other component to the one component after the detection of the transaction including the fault from the other component (see column 5 lines 45-53).

In regards to claim 22, Sonnier discloses:

wherein the one component is configured to not process the transaction including the fault (see column 5 lines 45-53).

In regards to claim 23, Sonnier discloses:

a plurality of redundant storage circuits configured to redundantly store digital data. Sonnier discloses identical CPUs each with a memory (see figure 1a items 12a, 12b; figure 2 items 22, 28 and column 14 lines 7-12 and 50-60).

In regards to claim 24, Sonnier discloses:

a plurality of mirror circuits individually configured to effect storage operations with respect to both of the storage circuits (see figure 1a and column 6 lines 5-25).

In regards to claim 25, Sonnier discloses:

wherein the one component is configured to disable an interface in communication with the other component to disable the communication of the subsequent transactions (see column 5 lines 45-53).

In regards to claim 26, Sonnier discloses:

wherein the one component is configured to communicate and process transactions with respect to an additional component after the disablement of the communication of the subsequent transactions. Sonnier discloses isolating a link or router element that introduced an error (see column 5 lines 45-53). Since only the faulty link or router element that caused the error is isolated, the one component would continue processing transactions with respect to an additional component after the disablement of the communication of the subsequent transactions.

In regards to claim 27, Sonnier discloses:

wherein at least one of the subsequent transactions does not include a fault. Sonnier discloses isolating a link or router element that introduced an error (see column 5 lines 45-53). If there is isolation, then all of the communications of subsequent transactions are disabled, including subsequent transactions that would not include a fault.

In regards to claim 28, Sonnier discloses:

storage circuitry comprising a plurality of redundant storage circuits configured to redundantly store digital data. Sonnier discloses identical CPUs each with a memory (see figure 1a items 12a, 12b; figure 2 items 22, 28 and column 14 lines 7-12 and 50-60).

a plurality of components coupled with the storage circuitry and the components are configured to communicate transactions with respect to one another and to process received transactions to effect operations with respect to storage of digital data using the redundant storage circuits (see figure 1a and column 10 lines 35-43 and column 7 lines 13-35);

wherein the components are individually configured to identify transactions which include a fault, and to prevent processing of the transactions which have been identified as including a fault using the respective individual component. Sonnier discloses the CRC of each message is checked at destination as well as while in route to the destination (ex. at each router crossing), indicating identifying transactions which include a fault (see column 5 lines 35-40). He further discloses isolating a link or a router element that introduces an error, indicating preventing processing of the transactions which have been identified as including a fault using the respective individual component (see column 5 lines 45-53).

In regards to claim 29, Sonnier discloses:

wherein the transactions which include a fault are communicated from at least one of the components, and others of the components are configured to disable communications with respect to the one component to prevent the processing (see column 5 lines 45-53).

In regards to claim 30, Sonnier discloses:

wherein the others of the components are individually configured to disable a respective interface coupled with the one component to disable the communications (see column 5 lines 45-53).

In regards to claim 31, Sonnier discloses:

wherein the transactions for which processing was prevented would have otherwise been processed by recipient components (see column 5 lines 45-53).

In regards to claim 32, Sonnier discloses:

wherein the components are individually configured to prevent the respective processing responsive to the identification (see column 5 lines 45-53)..

In regards to claim 33, Sonnier discloses:

wherein at least one of the components is configured to identify at least one of the transactions including a fault as being communicated from an other of the components and to prevent processing of subsequent transactions communicated from the other component after the identifying (see column 5 lines 45-53).

In regards to claim 34, Sonnier discloses:

wherein the one component is configured to process transactions from additional ones of the components after the identifying. Sonnier discloses isolating a link or router element that introduced an error (see column 5 lines 45-53). Since only the faulty link or router element that

caused the error is isolated, the one component would continue processing transactions from additional ones of the components after the identifying.

In regards to claim 35, Sonnier discloses:

means for redundantly storing digital data. Sonnier discloses identical CPUs each with a memory (see figure 1a items 12a, 12b; figure 2 items 22, 28 and column 14 lines 7-12 and 50-60).

plural means for processing transactions for effecting operations with respect to the redundant storage of digital data (see figure 1a and column 10 lines 35-43 and column 7 lines 13-35);

wherein one of the means for processing is identified responsive to communication of a transaction including a fault from the one means for processing, and wherein subsequent transactions communicated from the identified means for processing which would otherwise be processed are not processed by at least one other of the means for processing responsive to the identification. Sonnier discloses the CRC of each message is checked at destination as well as while in route to the destination (ex. at each router crossing), indicating identifying transactions including a fault from the one means for processing (see column 5 lines 35-40). He further discloses isolating a link or a router element that introduces an error, indicating wherein subsequent transactions communicated from the identified means for processing which would otherwise be processed are not processed by at least one other of the means for processing responsive to the identification (see column 5 lines 45-53).

In regards to claim 36, Sonnier discloses:

wherein the subsequent transactions individually do not include a fault. Sonnier discloses isolating a link or router element that introduced an error (see column 5 lines 45-53). If there is isolation, then all of the subsequent transactions are disabled, including subsequent transactions that would not include a fault.

In regards to claim 37, Sonnier discloses:

wherein the other means for processing comprises means for disabling communications with respect to the one means for processing responsive to the identification (see column 5 lines 45-53).

In regards to claim 38, Sonnier discloses:

wherein the other means for processing comprises means for processing transactions of additional means for processing after the identification. Sonnier discloses isolating a link or router element that introduced an error (see column 5 lines 45-53). Since only the faulty link or router element that caused the error is isolated, the one component would continue processing transactions from additional ones of the components after the identifying.

In regards to claim 39, Sonnier discloses:

storing digital data using a data storage system (see column 7 lines 13-35);

communicating a plurality of transactions intermediate a plurality of components of the data storage system (see figure 1a and column 10 lines 35-43);

processing the transactions using the components (see column 7 lines 13-35);

using the components, effecting operations with respect to storage of digital data responsive to the processing (see column 7 lines 13-35);

identifying one of the transactions from one of the components as including a fault. Sonnier discloses the CRC of each message is checked at destination as well as while in route to the destination (ex. at each router crossing), indicating identifying one of the transactions from one of the components as including a fault (see column 5 lines 35-40); and

disabling communications of others of the transactions from the one component responsive to the identifying. Sonnier further discloses isolating a link or a router element that introduces an error, indicating disabling communications of others of the transactions from the one component responsive to the identifying (see column 5 lines 45-53).

In regards to claim 40, Sonnier discloses:

wherein the storing digital data comprises redundantly storing digital data using a plurality of redundant storage circuits of the data storage system. Sonnier discloses identical CPUs each with a memory (see figure 1a items 12a, 12b; figure 2 items 22, 28 and column 14 lines 7-12 and 50-60).

In regards to claim 41, Sonnier discloses:

disabling respective interfaces of the other components responsive to the identifying (see column 5 lines 45-53).

In regards to claim 42, Sonnier discloses:

processing transactions using the other components after the disabling. Sonnier discloses isolating a link or router element that introduced an error (see column 5 lines 45-53). Since only the faulty link or router element that caused the error is isolated, the one component would continue processing transactions using the other components after the disabling.

In regards to claim 43, Sonnier discloses:

disabling communications of at least one of the others of the transactions not including a fault. Sonnier discloses isolating a link or router element that introduced an error (see column 5 lines 45-53). If there is isolation, then all of the communications of subsequent transactions are disabled, including transactions that would not include a fault.

In regards to claim 44, Sonnier discloses:

storing digital data using storage circuitry of a data storage system (see column 7 lines 13-35);

providing a plurality of redundant components of the data storage system and individually configured to effect data storage operations of the storage circuitry (see figure 1a and column 10 lines 35-43 and column 7 lines 13-35)

identifying corruption of one of the components (see column 5 lines 35-40);

isolating the one of the components responsive to the identifying (see column 5 lines 45-53); and

after the isolating, providing redundant functionality of the isolated component using a redundant one of the components corresponding to the isolated component (see column 6 lines 5-25).

In regards to claim 45, Sonnier discloses:

redundantly storing the digital data using a plurality of redundant storage circuits. Sonnier discloses identical CPUs each with a memory (see figure 1a items 12a, 12b; figure 2 items 22, 28 and column 14 lines 7-12 and 50-60).

In regards to claim 46, Sonnier discloses:

where the providing redundant functionality comprises providing a transaction using the redundant component and corresponding to an isolated transaction of the isolated component (see column 6 lines 5-25).

In regards to claim 47, Sonnier discloses:

wherein the redundant component provides the same functionality as functionality of the isolated component (see column 14 lines 7-12).

In regards to claim 48, Sonnier discloses:

preventing processing of transactions from the isolated component which would have otherwise been processed. Sonnier discloses isolating a link or a router element that introduces an error, indicating preventing processing of transactions from the isolated component, which would have otherwise been processed (see column 5 lines 45-53).

In regards to claim 49, Sonnier discloses:

disabling communications of others of the components with respect to the isolated component (see column 5 lines 45-53).

In regards to claim 50, Sonnier discloses:

disabling at least some communications from the isolated component (see column 5 lines 45-53).

In regards to claim 51, Sonnier discloses:

wherein the at least some communications individually do not include a fault. Sonnier discloses isolating a link or router element that introduced an error (see column 5 lines 45-53). If there is isolation, then all of the communications of subsequent transactions are disabled, including some communications individually do not include a fault.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C. Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ecp
7/12/05

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